Please delete the present Abstract of the Disclosure.

Please add the following amended Abstract of the Disclosure:

A semiconductor synchronous dynamic random access memory (SDRAM) device ~~is provided which is~~ capable of correcting ~~efficiently~~ bits having a low error rate in a Pause Refresh Tail distribution and of ~~greatly~~ reducing a data holding current by lengthening a refresh period so that the refresh period exceeds a period for a Pause Refresh real power. The semiconductor memory device is made up of a 16-bit SDRAM ~~(Synchronous Dynamic Random Access Memory)~~ having a Hamming Code and including an ECC (Error Correcting Code) circuit made up of ~~a~~ an encoding circuit ~~being~~ controlled by a first test signal to output ~~by arithmetic operations~~ a parity bit corresponding to an information bit, a decoding circuit ~~being~~ controlled by a second test signal to output an error location detecting signal indicating an error bit in ~~bits of~~ a codeword, and an error correcting circuit ~~being~~ controlled by a third test signal to input an error location detecting signal and to output an error bit in a reverse manner.